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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,154	04/01/2004	Blaine Douglas Gaither	10001399-2	7372

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EXAMINER	
ELLIS, KEVIN L	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,154	GAITHER, BLAINE DOUGLAS	
	Examiner	Art Unit	
	Kevin L. Ellis	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 1-4 is/are allowed.

6)☒ Claim(s) 5-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-22 are presented for examination. The current application is a continuation of application serial number 09/733,123, now U.S. Patent No. 6,721,848.

Claim Rejections – 35 USC § 103

2. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 5-11 and 13-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matick et al., U.S. Patent 6,081,872, in view of Kimmel et al., U.S. Patent 5,713,004, Handy, "The Cache Memory Book", 1993, and Motorola, "MC 88410 Secondary Cache Controller User's Manual".

A) As to claims 5, 8, 9, 19, and 20, Matick et al. discloses the invention substantially as claimed. Matick et al. teaches a method that includes intermediary caches for higher level caches (i.e. shared L2 cache see Fig 8), the intermediary cache being virtually addressed (see Col 5 Lines 22-35). However, Matick does not disclose using a coherency protocol. Kimmel et al. teaches it was common to use coherency protocols in systems that contained multiple processors, caches, and shared L2 caches (see Col 1 Lines 31 to Col 2 Line 10). As taught by Kimmel et al. these protocols typically used a coherency status bit that included a Modified, Exclusive, Shared, and Invalid states. This was

needed to maintain coherency of data between the various processors and caches. Accordingly it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Kimmel et al. in the system of Matick et al. and provide a coherency protocol such as that taught by Kimmel et al. in order to maintain coherency of data among the various processors and caches. Kimmel et al. also teaches snooping for maintaining the coherency of the data. The coherency protocol and status bits used make the cache operate as a "coherency filter". This snoop processing of the intermediary cache would initiate further snoop processing on higher level caches based on the results of snooping the intermediary caches. It was common in the art to "filter out" snoops at the L2 cache level and not send them to the L1 caches when there was no snoop hit in the L2 cache. If the L2 cache is inclusive and there isn't a snoop hit at the L2 level, then there could not be a snoop hit at the L1 level so there is no need in having the snoop operation performed by the L1 cache. Kimmel specifically states the hardware used. The L1 cache is part of the microprocessor MC88110 (see Col 1 Lines 50-55) and the L2 cache is the MC88410 (see Col 2 Lines 6-10). Kimmel states that the "MC88410 Secondary Cache Controller User's Manual" on pages 2-41 to 2-72 teaches the snoop protocol used. Page 2-41 of the MC88410 manual discusses the snoop protocol and states that once snooping has occurred at the MC88410 level, "the MC88410 must determine whether the MC8810 must be notified of the snooped transaction" (see P 2-41). Thus the MC88410 performs the "snoop filtering" of the claimed invention. Matick et al. also does not explicitly state that the L1 and L2 cache are inclusive (i.e. all data contained in the L1 caches are in the L2 caches). It can be

argued that this is an inherent feature of Matick et al.. In order for the cache to be non-inclusive addition steps and/or information must be stored in order for the caches to know where a piece of data is located in order to maintain coherency. These additional steps and/or information would be described in the patent if Matick et al. taught a non-inclusive cache design. However, there are advantages to have an inclusive cache design. As taught by Handy, the L2 cache can prescreen invalidation cycles before they are passed to the L1 cache when the data is inclusive (see P 250). This reduces the number of access requests to the L1 cache allow it to service more requests to the processor. Accordingly, it would have been obvious to operate the caches of Matick et al. in an inclusive manner for the reasons given by Handy.

B) As to claims 6, 10, and 21, it is inherent that in order for the intermediary cache to be inclusive of all data in the higher level caches that the capacity of the intermediary cache exceed a total capacity of all corresponding higher level caches.

C) As to claims 7, 11, and 22, in order to maintain inclusion it is inherent that data that's evicted from an intermediary cache would also have to be evicted from a higher level cache, otherwise inclusion would not be maintained.

D) As to claim 13, the architecture of Matick and Kimmel would operate the intermediary caches as a coherency filter by filtering out unnecessary snoop requests.

E) As to claims 14 and 15, the intermediary cache of Matick et al. is a shared cache (i.e. a shared L2 cache) and there is a hierarchy of local caches and intermediary caches.

F) As to claims 16-18, Matick et al. discloses the invention substantially as claimed. However, Matick et al. does not specifically indicate the structure of the physical

interconnect. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize various commonly used types of interconnects, such as the claimed bus, point-to-point link, or cross-bar connection. These are all common interconnects used in computer systems to connect the various elements.

4. Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Matick et al., U.S. Patent 6,081,872, in view of Kimmel et al., U.S. Patent 5,713,004, and Handy, "The Cache Memory Book", 1993, and Guy, U.S. Patent 5,778,424.

A) As to claim 12, Matick et al. discloses the invention substantially as claimed. However, Matick et al. does not disclose using a prefetch status bit when prefetching data. Guy teaches the use of a prefetch status bit (see Col 15 Lines 17-28) which is used to indicate when the next sequential address should be prefetched. This can increase the hit ratio of the cache for sequential accesses. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Guy in the system of Matick et al. and provide prefetch status bits in order to indicate when data should be prefetched for the advantages stated above.

Allowable Claims

5. Claims 1-4 are allowed.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin L. Ellis whose telephone number is 571-272-4205. The examiner can normally be reached on weekdays from 6:00AM-2:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Kevin L. Ellis
Primary Examiner
December 10, 2004